Interfacing the LTC1094 to a Parallel Bus

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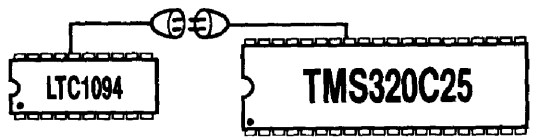

Introduction

This application note describes the hardware and software required to interface the LTC1094 10-bit data acquisition system to the TMS320C25 digital signal processor. The circuitry shown can be used to interface any member of the LTC1090 family to the bus of virtually any processor with only minor modifications. The software provided is specific to the TMS320 family. The interface shown can be either interrupt driven or polled by the processor after a convert command has been given to the LTC1094. The interface is capable of completing a 10-bit conversion and transferring the data to the TMS320C25 in 40μs. Configuration of the LTC1094 and the TMS320C25 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be discussed. Finally, a summary of results will be provided.

Interface Details

The LTC1094 is a serial 10-bit data acquisition system. It uses a half duplex synchronous serial interface. It uses a D_{IN} word to configure the A/D for channel number, unipolar or bipolar, and MSB first or LSB first. Data is shifted out on the D_{OUT} line. Both D_{IN} and D_{OUT} are synchronous with the CLK line.

Many processors do not have a compatible serial port. It then becomes necessary to construct an interface circuit that will allow the LTC1094 to hang directly on the data bus of the processor. The circuit of Figure 1 interfaces directly to the TMS320C25 bus. It latches the D_{IN} word provided by the processor and then shifts it to the LTC1094. The LTC1094 then clocks out the D_{OUT} word to a shift register where the data is latched and the conversion complete signal is sent to the processor. When the processor requests the D_{OUT} word the interface circuit comes out of tri-state and the data is present on the bus. The circuit generates the clock for the LTC1094 and automatically shuts it off after the conversion has been done. The processor must provide chip select, read/write and interrupt lines as well as a 16-bit data bus. (For an 8-bit data bus a two byte read would be required.) When the read/write line is LOW and the chip select line is LOW the D_{IN} word is latched into the 74LS165. When the read/write line is HIGH and the chip select line is LOW the D_{OUT} word is read from the 74LS365 tri-state buffers.

Hardware Description

The DSP was emulated and the code for this interface was developed on a TMS320C25 Software Development System (SWDS).

The timing diagram of Figure 2 was obtained with an HP1631 logic analyzer with an LTC1094 CLK frequency of 500kHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1094 please see the data sheet.

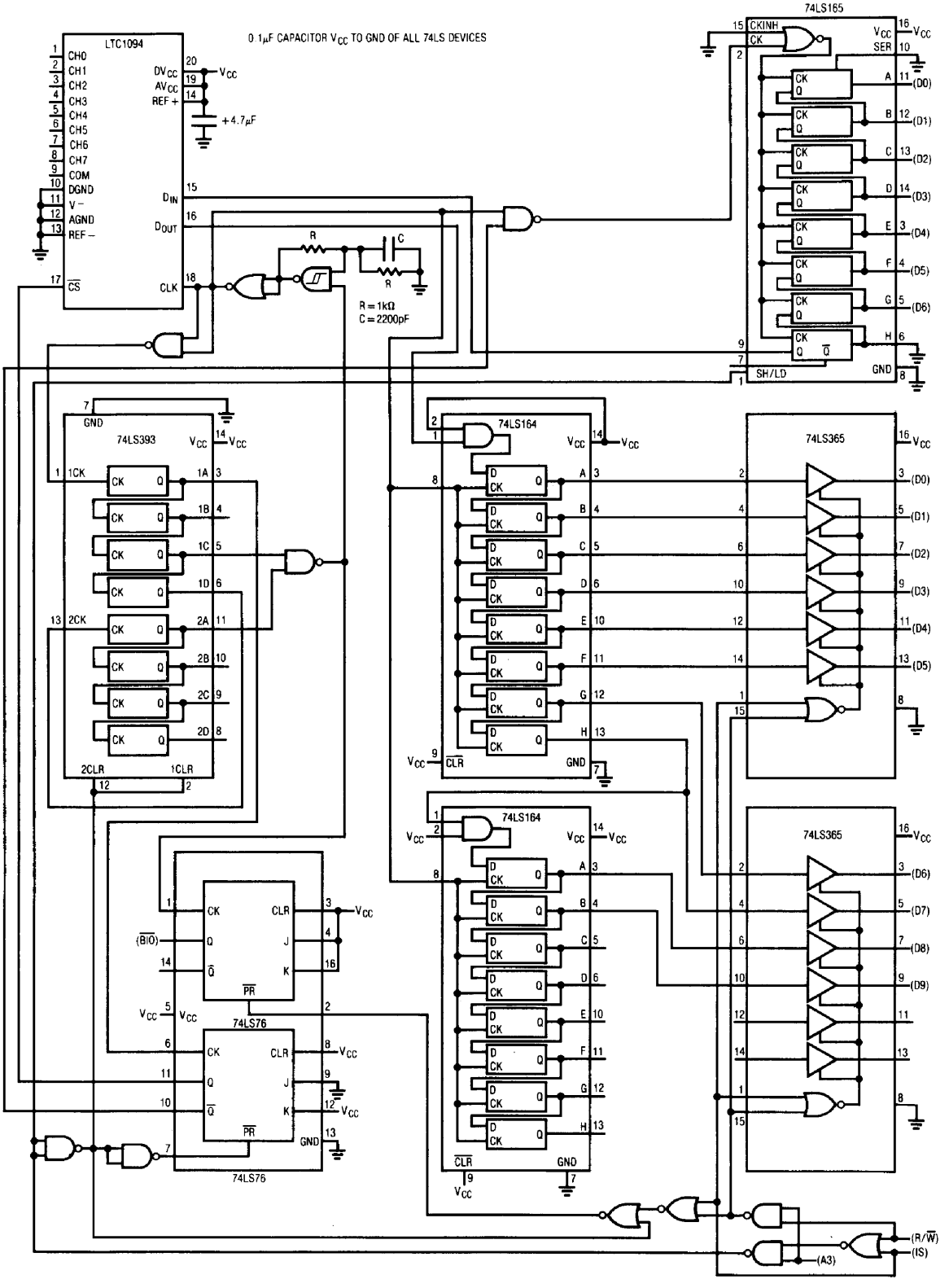

Figure 1. Circuit Allows LTC1094 to Interface Directly with the TMS320C25 Data Bus

Software Description

The software outputs a D_{IN} word from the TMS320C25 to the interface and when informed by the interface that the resulting data is present reads in the D_{OUT} word of the LTC1094.

The code of Figure 5 first disables all interrupts. Next, a D_{IN} word is placed in >60 of the TMS320C25 as shown in Figure 3. This D_{IN} word configures the LTC1094 for CH7 with respect to COM, unipolar, and MSB first. This D_{IN} word is then output to Port 8 of the TMS320C25. The software then polls the $\overline{BIO}$ pin until the interface pulls it LOW indicating that the conversion is complete and that the data is ready to be received by the TMS320C25. (The interface could just as easily connect to one of the maskable interrupt pins so that the processor could be performing some task while waiting for the conversion to be completed.) The data is then read into the TMS320C25 and placed into >61. The data at this point is right justified as shown in Figure 4.

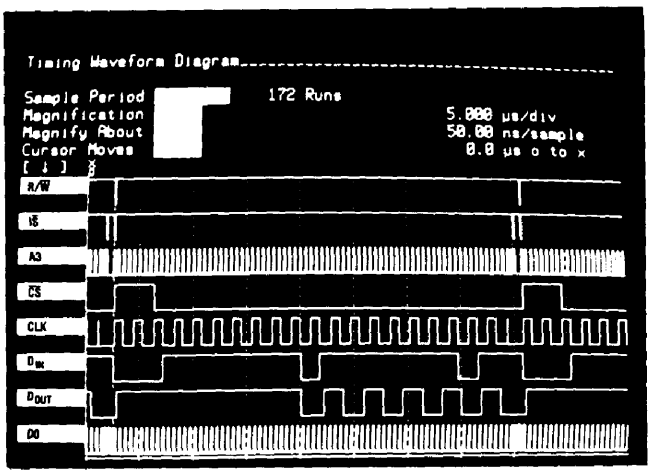

Figure 2. Timing Diagram Shows 25kHz Throughput Rate

Summary

An interface between the LTC1094 and the TMS320C25 with a combined data conversion and transfer rate of 40μs was demonstrated. This inexpensive interface (about $2.00 in production quantities) uses ten 74LS chips to allow the LTC1094 to hang directly on the data bus of the TMS320C25. The circuit shown here should work with any 16-bit processor (an 8-bit processor would require two reads per conversion) that has a read/write line, and external interrupt capability.

0	1	1	1	1	1	1	1	
NULL	START	S/D	O/S	SEL1	SEL0	UNI	MSBF	>60

Figure 3. D_{IN} Word for LTC1094

MSB														LSB
X	X	X	X	X	X	9	8	7	6	5	4	3	2	1	0

Figure 4. D_{OUT} of LTC1094 Stored in >61 of TMS320C25

LABEL	CODE	MNEMONIC	COMMENTS
		AORG>20	
START	CE01	DINT	DISABLE INTERRUPTS
LOOP	CAFF	LACK >7F	D_{IN} FOR LTC1094
	6060	SACL >60	PUT D_{IN} IN >60
	E860	OUT >60.8	OUTPUT D_{IN} TO PORT 8
WAIT1	FA80005F	BIOZ READ	IF DONE GO TO READ
	FF800024	B WAIT1	IF NOT DONE GO TO WAIT1
		AORG >5F	
READ	8861	IN >61.8	PUT D_{OUT} IN >61

Figure 5. TMS320C25 Code for Interfacing to LTC1094